Course Code: 20EC4201 **R20**

SIDDHARTH INSTITUTE OF ENGINEEERING & TECHNOLOGY:: PUTTUR

Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code: VLSITechnology(20EC4201)

Course & Branch: M.Tech-VLSI

Year & Sem: I-M.Tech& I-Sem

Regulation: R20

UNIT–I

REVIEW OFMICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES

1.	a)	Explain different steps involved in preparation CMOS using twin tub process.	[L2][CO1]	**[8M]**
	b)	Define Figure of merit and g_{ds}.	[L1][CO1]	**[4M]**
2.		Derive the relation between drain to source current I_{ds}VS drain to source voltage V_{ds} in non saturated and saturated.	[L4][CO1]	**[12M]**
3.	a)	Compare CMOS and Bi-CMOS.	[L2][CO1]	**[7M]**
	b)	Write short notes on latch-up in CMOS circuits.	[L2][CO1]	**[5M]**
4.		Determine the Pull-up and Pull-down ratio for NMOS inverter through one (or) more pass transistors.	[L5][CO1]	**[12M]**
5.	a)	What is meant by body effect?	[L2][CO1]	**[6M]**
	b)	Explain a Bi-CMOS inverter with a neat sketch.	[L2][CO1]	**[6M]**
6.	a)	Illustrate the main steps in a typical N-WELLprocess.	[L2][CO1]	**[6M]**
	b)	Briefly discuss about the pass transistor.	[L2][CO1]	**[6M]**
7.	a)	Compare NMOS and CMOS technology.	[L2][CO1]	**[6M]**
	b)	Derive the expression for ZPU/ZPD.	[L4][CO1]	**[6M]**
8.	a)	Define the term Threshold voltage of MOSFET and explain its significance	[L1][CO1]	**[6M]**
	b).	Explain the NMOS depletion mode transistor.	[L2][CO1]	**[6M]**
9	a)	Explain about the Structure of NMOS transistor	[L2][CO1]	**[8M]**
	b)	Explain the operation ofCMOS inverter with a logic diagram.	[L2][CO1]	**[4M]**
10	a)	Explain about NMOS inverter with neat sketch	[L2][CO1]	**[6M]**
	b)	Define electrical properties of MOS circuits.	[L2][CO1]	**[6M]**

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UNIT –II

LAYOUTDESIGN AND TOOLS\LOGICGATES &LAYOUTS

1.	a)	Explain how stick diagrams can be used for layout diagrams.	[L1][CO2]	**[8M]**
	b)	Discuss the wiring capacitance	[L6][CO2]	**[4M]**
2.	a)	Explain about static complementary gates.	[L2][CO2]	**[6M]**
	b)	What are the different strategies for building low power gates?Explain.	[L1][CO2]	**[6M]**
3.	a)	Differentiate switch logic and gate logic. .	[L4][CO2]	**[6M]**
	b)	List the salient features of sub system layout.	[L1][CO2]	**[6M]**
4.	a)	Explain clearly the Scalable design rules.	[L2][CO2]	**[6M]**
	b)	Explain clearly Wires and Vias in VLSIdesign	[L2][CO2]	**[6M]**
5.		Design the static complementary pull-up and pull-down networks for AOI expression	[L6][CO2]	**[12M]**
6.		Define the following terms .		
	a)	Speed power product.	[L1][CO2]	**[5M]**
	b)	Delay through RC transition time	[L1][CO2]	**[7M]**
7.	a)	Explain briefly about Resistive Inter-Connect delay and RC Trees delay	[L2][CO2]	**[6M]**
	b)	Explain about driving large loads with diagram	[L2][CO2]	**[6M]**
8.		What are layout design rules?Explain the layer representations and based design rules for CMOS process.	[L1][CO2]	**[12M]**
9.	a)	Implement NANDgate inNMOS technology and hence draw its stick diagram anddesign a layout for the stick diagram	[L3][CO2]	**[6M]**
	b)	Discuss about the effects of scaling down the dimensions of MOS circuits and Systems.	[L6][CO2]	**[6M]**
10.	a)	Explain switch Logic and Alternative Logic.	[L2][CO2]	**[6M]**
	b)	Briefly discuss about the combinational logic function.	[L2][CO2]	**[6M]**

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UNIT –III

COMBINATIONALLOGICNETWORKS\SEQUENTIALSYSTEMS

1.	a)	Explain in detail about the requirements in designing logic networks using realistic interconnect models	[L2][CO3]	**[6M]**
	b)	Draw the single row layout design.	[L2][CO3]	**[6M]**
2.	a)	Explain briefly about power optimization.	[L2][CO3]	**[6M]**
	b)	Draw the switch implementation of a multiplexer	[L2][CO3]	**[6M]**
3.	a)	Briefly discuss about crosstalk minimization	[L2][CO3]	**[6M]**
	b)	Briefly discuss about Fanout with diagram.	[L2][CO3]	**[6M]**
4.	a)	Write short notes on power optimization of combinational logic networks.	[L1][CO3]	**[6M]**
	b)	Explain path delay with respect to combination networks delay.	[L2][CO3]	**[6M]**
5.	a)	Explain the clocking disciplines and power optimization in sequential systems.	[L2][CO3]	**[6M]**
	b)	What are the various simulators used for combinational logic?	[L1][CO3]	**[6M]**
6.	a)	Explain clearly about switch simulation.	[L2][CO3]	**[6M]**
	b)	Explain about the combinational network testing.	[L2][CO3]	**[6M]**
7.		Draw the layout diagram of three input NAND gate in CMOS.	[L2][CO3]	**[12M]**
8.		What is simulation? Explain about various types of simulation applied at different levels of fabrication.	[L1][CO3]	**[12M]**
9.	a)	With suitable examples explain about network delays combinational logic circuits.	[L2][CO3]	**[6M]**
	b)	Implement an ‘n-bit’shift register and explain its operation over one clock cycle	[L3][CO3]	**[6M]**
10.	a)	Discuss briefly about standard cell layout design.	[L6][CO3]	**[6M]**
	b)	Briefly explain the block diagram of phase locked loop for clock generation	[L2][CO3]	**[6M]**

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UNIT-IV

FLOORPLANNINGAND ARCHITECTUREDESIGN

1.	a)	Briefly discuss about floor planning methods.	[L2][CO4]	**[6M]**
	b)	Draw and explain the block placement and channel definition	[L2][CO4]	**[6M]**
2.	a)	Write a short notes on global routing.	[L1][CO4]	**[6M]**
	b)	Explain the concept of switch box routing	[L2][CO4]	**[6M]**
3.	a)	Discuss about different floor planning tips.	[L6][CO4]	**[6M]**
	b)	Write a short notes on design validation.	[L1][CO4]	**[6M]**
4.	a)	Explain about placement and routing at chip level design	[L2][CO4]	**[6M]**
	b)	Explain about architecture testing	[L2][CO4]	**[6M]**
5.	a)	Discuss about off-chip connections and packages.	[L6][CO4]	**[8M]**
	b)	Draw and explain the power line inductance	[L2][CO4]	**[6M]**
6.	a)	Draw and explain the I/O architecture with a neat sketch	[L2][CO4]	**[6M]**
	b)	Explain the concept of pad design with a diagram.	[L2][CO4]	**[6M]**
7.		Explain the concept of register transfer design with data path control architecture	[L2][CO4]	**[12M]**
8.		With a flowchart explain the concept of ASM chart design.	[L2][CO4]	**[12M]**
9.	a)	Discuss high level synthesis.	[L6][CO4]	**[6M]**
	b)	Write a short notes on power down modes.	[L1][CO4]	**[6M]**
10.	a)	Explain the architecture for low power with a diagram.	[L2][CO4]	**[6M]**
	b)	Write a notes on linear feedback shift register.	[L2][CO4]	**[6M]**

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UNIT-V

INTRODUCTION TO CADSYSTEM AND CHIPDESIGN

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1.		Write about the following.		
	a)	Hardware-software co-design.	[L2][CO5]	**[6M]**
	b)	Floor planning methods	[L2][CO5]	**[6M]**
2.	a)	Write a short notes on layout synthesis.	[L2][CO5]	**[6M]**
	b)	Discuss about global routing.	[L6][CO5]	**[6M]**
3.	a)	With an example give the method involved in the chip design	[L2][CO5]	**[8M]**
	b)	Briefly discuss about CAD system	[L2][CO5]	**[4M]**
4.	a)	Explain about system on chips and embedded CPUs.	[L2][CO5]	**[6M]**
	b)	Write a notes on logic synthesis.	[L2][CO5]	**[6M]**
5.		With a diagram explain about detailed routing method.	[L2][CO5]	**[12M]**
6.	a)	Explain the timing analysis and optimization process.	[L2][CO5]	**[6M]**
	b)	Write about test generation pattern.	[L2][CO5]	**[6M]**
7.	a)	Explain the technology independent logic optimization.	[L2][CO5]	**[8M]**
	b)	Draw the diagram of irredundant-reduced cycle.	[L2][CO5]	**[4M]**
8.	a)	Write a short notes on sequential machine optimizations.	[L1][CO5]	**[6M]**
	b)	Explain about scheduling ad binding.	[L1][CO5]	**[6M]**
9	a)	Write about switch level simulation.	[L1][CO5]	**[4M]**
	b)	Write a short notes on chip level placement.	[L1][CO5]	**[8M]**
10.		Explain about technology dependent logic optimization.	[L2][CO5]	**[12M]**

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